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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,023	02/24/2004	Iosif R. Korsunsky		3891

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EXAMINER	
TSUKERMAN, LARISA Z	
ART UNIT	**PAPER NUMBER**
2833	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,023	KORSUNSKY ET AL.	
	Examiner	Art Unit	
	Larisa Z Tsukerman	2833	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 13-15* is/are rejected.

7)☒ Claim(s) *5,10-12,16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (6497580).

Watanabe et al. disclose a method for electrically interconnecting two printed circuit boards comprising the steps of:

providing a first printed circuit board 7;

providing a second printed circuit board 13;

providing a receiving slot 15 in one of the first 7 and the second printed circuit boards such that the first 7 and the second 13 printed circuit boards are orthogonally intersected with each other (see Fig.1); and

providing at least one electrical connector 22 adjacent the receiving slot 15 and in electrical connection with the first and the second printed circuit boards (see Col.7, lines 40-57).

Claims 1 – 4, 6-9 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Lauchner et al. (5190462).

In regard to claim 1, Lauchner et al. disclose a method for electrically interconnecting two printed circuit boards comprising the steps of:

providing a first printed circuit board 30;

providing a second printed circuit board 50;

providing a receiving slot 42 and 58 in one of the first 30 and the second 50 printed circuit boards such that the first 30 and the second 50 printed circuit boards are orthogonally intersected with each other (see Fig.4); and

providing at least one electrical connector 80 adjacent the receiving slot 42 and in electrical connection with the first and the second printed circuit boards.

In regard to claim 2, Lauchner et al. disclose the first 30 and the second 50 printed circuit boards together define **four** quadrants (see Fig.7A-C).

In regard to claim 3, Lauchner et al. disclose the at least one electrical connector 80 comprises a first connector arranged in a first quadrant and a second connector 80 arranged in a fourth quadrant (see Fig 7B).

In regard to claim 4, Lauchner et al. disclose the first and the second connectors 80 are mounted on the second printed circuit board 50.

In regard to claim 6, Lauchner et al. disclose a method for electrically interconnecting multiple printed circuit boards, comprising the steps of:

providing a plurality of first printed circuit boards 50;

providing a plurality of second printed circuit boards 30;

providing receiving slots 58 and 42 in either the first printed circuit boards or the second printed circuit boards such that the first and the second printed circuit boards are orthogonally intersected with each other (see Fig.4), every two orthogonally

arranged printed circuit boards together defining four quadrants Q1-Q4 (see Figs. 7A-C); and

providing, in at least one of the four quadrants of every two orthogonally arranged printed circuit boards 50 and 30, a respective electrical connector 80 to electrically intercormect the first and the second printed circuit boards.

In regard to claim 7, Lauchner et al. disclose the receiving slot 42 is defined in the first printed circuit board 30.

In regard to claim 8, Lauchner et al. disclose the first and the second quadrants Q1-2 of every two orthogonally arranged printed circuit boards each have the electrical connector 80 arranged therein, and each connector is mounted on the second printed circuit board 50 (see Fig.7A-C).

In regard to claim 9, Lauchner et al. disclose the connectors 70 and 96 respectively arranged in the first and the second quadrants are mirror image with respect to the second printed circuit board 50.

In regard to claim 13, Lauchner et al. disclose a method for configuring an electrical system 14 adapted for mating with a complementary device 12, comprising the steps of:

providing a printed circuit board 30 having a first surface;

providing a first group of conductive traces 100 (see Fig.7C) on the surface;

providing a second group of conductive traces 102 on the surface and spaced from the first conductive traces 100;

mounting a first electrical connector 96 on the first group of the conductive traces 100, the first electrical connector 96 defining a mating face; and

mounting a second electrical connector 98 on the second group of the conductive traces 102, the second electrical connector 98 defining a second mating face facing the first mating face (see Fig.2).

In regard to claim 14, Lauchner et al. disclose a method of making an interconnection system 14, comprising steps of:

providing a first set of parallel spaced printed circuit boards 30 defining first front edge sections (not marked, see in Fig.4 edges near numerals 42 and 43) thereof, respectively;

providing a second set of parallel spaced printed circuit boards 50 defining second front edge sections (not marked, see in Fig.4 edges near numerals 55 and 58) thereof, respectively; and

intersecting each of the first set of parallel spaced printed circuit boards 30 with all of the second set of parallel spaced printed circuit boards 50, respectively, around the first front edge section of the each of the first set of parallel spaced printed circuit boards 30 and the second front edge sections of the second set of parallel spaced printed circuit boards 50.

In regard to claim 15, Lauchner et al. disclose the method further including a step of providing at least one electrical connector 80 located in one of four quadrants derived from intersection by the each of the first set of parallel spaced printed circuit boards 30 and the corresponding one of the second set of parallel spaced printed circuit boards 50, and electrically connected to the each of the first set of parallel spaced printed circuit boards 30 and the corresponding one of the second set of parallel

spaced printed circuit boards 50 (see Fig.4 and 7A-C).

Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Cabourne (US 4,904,197)

Cabourne discloses a method for configuring an electrical system adapted for mating with a complementary device, comprising the steps of:

providing a printed circuit board 14 having a first surface;

providing a first group of conductive traces 78 (see Fig.11, left) on the surface;

providing a second group of conductive traces 78 (right) on the surface and spaced from the first conductive traces;

mounting a first electrical connector 22 on the first group of the conductive traces 22, the first electrical connector 22 defining a mating face (side with terminals 28); and

mounting a second electrical connector 24 on the second group of the conductive traces 78, the second electrical connector 24 defining a second mating face facing the first mating face (see Fig.2).

Allowable Subject Matter

Claims 5, 10 -12 and 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regard to claim 5, The method as recited in claim 4, wherein the first and the second electrical connectors each comprise an electrical contact and **an actuator** capable of actuating the contact to have a wiping contact with the first and the second printed circuit boards.

In regard to claims 10 – 12, The method as recited in claim 9, wherein the third and the fourth quadrants of every two orthogonally arranged printed circuit boards each have the electrical connector arranged therein.

11. The method as recited in claim 10, wherein the connectors respectively arranged in the third and the fourth quadrants are mirror image with respect to the second printed circuit board.

12. The method as recited in claim 11, wherein the connectors respectively arranged in the first and the fourth quadrants are mirror image with respect to the first printed circuit board.

In regard to claim 16, The method as recited in claim 15, wherein the connector 80 extends in a plurality of juxtaposed contacts therein, and the longitudinal direction with a plurality longitudinal direction is parallel to a center line defined by the four quadrants.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larisa Z Tsukerman whose telephone number is (571)-272-2015. The examiner can normally be reached on Monday through Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paula A Bradley can be reached on (571)-272-2800 ex. 33. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LT, 10/29/2004

THO D. TA
PRIMARY EXAMINER